ABSTRACT OF THE DISCLOSURE

A nonvolatile semiconductor memory device includes a memory array, a selecting circuit, a storage device, a power generator, a connecting circuit, and a write or erase controller. The selecting circuit selects one of memory cells from the memory array. A sequence for controlling write and erase operations for the memory cells is stored in the storage device. The power generator is able to generate certain voltage higher than requirement voltage for write or erase operation. The sequence includes a plurality of sub-sequences in which write or erase operation to the memory cell is implemented. Each of the sub-sequences includes before the end: a voltage resetting step of resetting a voltage impressed on the selecting circuit to the power voltage or grounding; and a route resetting step of resetting a switch of a transistor of the selecting circuit to last status just before write or erase operation.